Please type a plus sign (+) inside this box → ⊞

UTILITY PATENT APPLICATION TRANSMITTAL *(Only for new non-provisional applications under 37 CFR 1.53(b))*	Attorney Docket No.	BONN-039	Total Pages 17
	First Named Inventor or Application Identifier		
	Sghaier NOURY		
	Express Mail Label No.		

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, D.C. 20231

1. ☒ Fee Transmittal Form (submit an original, and a duplicate for fee processing)

2. ☒ Specification Total pages: 11
(preferred arrangement set forth below)
- Descriptive title of the invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R&D
- References to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (*if filed*)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. ☒ Drawing(s) (35 U.S.C. § 113) Total pages: 4

4. ☒ Oath or Declaration Total pages: 2

   a. ☒ Newly executed (original or copy)

   b. ☐ Copy from a prior application (37 C.F.R. 1.63(d))
   (for continuation/divisional with Box 17 completed)
   (Note Box 5 below)

      i. ☐ DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).

5. ☐ Incorporation by Reference (*useable if Box 4b is checked*). The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ☐ Microfiche Computer Program (*Appendix*)

7. Nucleotide and/or Amino Acid Sequence Submission
(*if applicable, all necessary*)

   a. ☐ Computer Readable Copy

   b. ☐ Paper Copy (identical to computer copy)

   c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ☒ Assignment Papers (cover sheet & document(s))

9. ☐ 37 C.F.R. 3.73(b) Statement (*when there is an assignee*) ☐ Power of Attorney

10. ☐ English Translation Document (*if applicable*)

11. ☐ Information Disclosure Statement (IDS) PTO-1449 ☐ Copies of IDS Citations

12. ☒ Preliminary Amendment

13. ☒ Return Receipt Postcard (MPEP 503) (*Should be specifically itemized*)

14. ☒ Small Entity Statement(s) ☐ Statement filed in prior application, Status still proper and desired

15. ☐ Certified copy of Priority Document(s) (*if foreign priority is claimed*)

16. ☐ Other:

17. If a **CONTINUING APPLICATION**, *check appropriate box and supply the requisite information:*

☐ Continuation ☐ Divisional ☐ Continuation-in-Part (CIP)

of prior application No.

18. CORRESPONDENCE ADDRESS

☐ Customer Number or Bar Code Label or ☒ Correspondence address below

NAME	James C. Lydon				
ADDRESS	100 Daingerfield Road Suite 100				
CITY	Alexandria,	STATE	VA	ZIP CODE	22314
COUNTRY	U.S.A.	TELEPHONE	703- 838-0445	FAX NO.	703- 838-0447

SIGNATURE OF ATTORNEY OR AGENT

NAME	James C. Lydon, Reg. No. 30,082
SIGNATURE	James C. Lydon
DATE	October 30, 2000

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Sghaier NOURY et al.

Serial Number: Not Yet Assigned

Filed: October 30, 2000

For: FUNCTIONAL REPLICATOR OF A SPECIFIC INTEGRATED CIRCUIT AND ITS USE AS AN EMULATION DEVICE

FEE TRANSMITTAL FORM

Commissioner for Patents
Washington, D.C. 20231

October 30, 2000

Sir:

The filing fee for this application is calculated as shown below:

	Number Filed	Number Extra	Rate	Basic Fee $ 710.00
Total Claims	13 - 20		* x 18.00	
Independent Claims	1 - 3		* x 80.00	
Multiple Dependent Claims			+ 270.00	+
Reduction by 1/2 for small entity				- 355.00
Fee for recording enclosed Assignment				40.00
TOTAL FEE				= $ 395.00

__ Payment of the filing fee is deferred.

XX Checks in the amount of $ 355.00 and 40.00 are attached.

XX Please charge any additional required fees or credit any overpayment to our Deposit Account No. 50-1258. Two copies of this Fee Transmittal are enclosed herewith.

Respectfully submitted,

James C. Lydon
Reg. No. 30,082

Attorney Docket No.: BONN-039
100 Daingerfield Road, Suite 100
Alexandria, VA 22314
Telephone: (703) 838-0445
Facsimile: (703) 838-0447

SMALL ENTITY DECLARATION

APPLICANT OR PATENTEE EUROPE TECHNOLOGIES S.A.

SERIAL NO. _____ ☐ PATENT NO _____ DOCKET NO. BONN-039

(Check one of blocks 1 or 2)

1. ☐ FILED OR ISSUED _____
2. ☒ SUBMITTED HEREWITH _____

FOR Functional replicator of a specific integrated circuit and its use as an emulation device
(Insert Title)

I(we) hereby declare that I(we) am(are) entitled to the benefit of small entity status with respect to the above-identified application or patent for purposes of paying reduced fees under 35 USC 41(a) & (b) to the U.S. Patent and Trademark Office.

☐ A. INDEPENDENT INVENTOR
I(we) qualify as (an) independent inventor(s) as defined in 37 CFR 1.9(c).

☐ B. INDIVIDUAL NON-INVENTOR
I would qualify as an independent inventor as defined in 37 CFR 1.9(c) if I had made the invention.

☒ C. SMALL BUSINESS CONCERN
I am ☐ THE OWNER ☐ AN OFFICIAL of the small business concern identified below and am empowered to act on behalf of the concern. The concern qualifies under 37 CFR 1.9(d) and 13 CFR 121.1301-1305. Rights under contract or law have been conveyed to and remain with the concern and are exclusive unless a checkmark is placed here ☐. All other rights belong to small entities as defined in 37 CFR 1.9.

☐ D. NON-PROFIT ORGANIZATION
I am an official am empowered to act on behalf of the non-profit organization identified below. The organization qualifies under 37 CFR 1.9(e), sub section: ☐ (1) ☐ (2) ☐ (3) ☐ (4). Rights under contract or law have been conveyed to and remain with the organization and are exclusive unless a checkmark is placed here ☐. All other rights belong to small entities as defined in 37 CFR 1.9.

I(we) acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b)).

I(we) declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

A. INDEPENDENT INVENTOR(S) B. INDIVIDUAL NON-INVENTORS

Name	Signature	Date
Name	Signature	Date
Name	Signature	Date

C. BUSINESS CONCERN D. NON-PROFIT ORGANIZATION

EUROPE TECHNOLOGIES S.A.
Name of Concern or Organization

Sghaier NOURY
Name of Person Signing

C.E.O.
Title

Les Taissounières HB3
Address 1681, Route des Dolines
06560 SOPHIA ANTIPOLIS - FRANCE

Signature S.NOURY

Date 18/10/00

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Sghaier NOURY et al.

Serial Number: Not Yet Assigned

Filing Date: October 30, 2000

For: FUNCTIONAL REPLICATOR OF A SPECIFIC INTEGRATED CIRCUIT AND ITS USE AS AN EMULATION DEVICE

TRANSMITTAL OF SMALL ENTITY DECLARATION

Commissioner for Patents
Washington, D.C. 20231

October 30, 2000

Sir:

The assignee of this Application claims small entity status as provided under 37 C.F.R. §1.9. A Small Entity Declaration for the U.S. patent application identified above is attached hereto.

Respectfully submitted,

James C. Lydon
Reg. No. 30,082

Atty. Docket No.: BONN-039
100 Daingerfield Road
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Facsimile: (703) 838-0447

Enclosure: Small Entity Declaration

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Sghaier NOURY et al.

Serial Number: Not Yet Assigned

Filing Date: October 30, 2000

For: FUNCTIONAL REPLICATOR OF A SPECIFIC INTEGRATED CIRCUIT AND ITS USE AS AN EMULATION DEVICE

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

October 30, 2000

Sir:

Please amend this new patent application, prior to calculation of the filing fee, as follows:

IN THE CLAIMS:

Please amend claims 4, 6, 9, 10, 12 and 13 as follows:

Claim 4, line 1, delete "or 3".

Claim 6, line 1, change "any one of claims 1 to 5" to -- claim 1 --.

Claim 9, line 1, delete "or 8".

Claim 10, line 1, change "any one of claims 1 to 9" to -- claim 1 --.

Claim 12, line 1, change "any one of claims 1 to 7" to -- claim 1 --.

Claim 13, line 1, change "any one of claims 1 to 7" to -- claim 1 --.

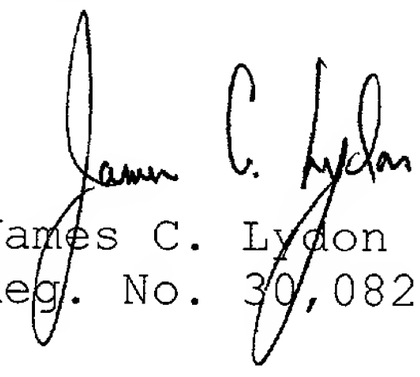
REMARKS

This Preliminary Amendment amends claims 4, 6, 9, 10, 12 and 13 by eliminating multiple dependencies. Claims 1-13 are pending.

A Recordation Form Cover Sheet and Transmittal of Small Entity Declaration are attached.

It is not believed that any fee is required for entry and consideration of this Preliminary Amendment. Nevertheless, the Commissioner is authorized to charge our Deposit Account No. 50-1258 in the amount of any such required fee.

Respectfully submitted,



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Facsimile: (703) 838-0447

Enclosures:
Recordation Form Cover Sheet
Transmittal of Small Entity Declaration

Functional replicator of a specific integrated circuit and its use as an emulation device

Technical field

The present invention relates generally to the prototyping, the development and the emulation of specific integrated circuits intended to be incorporated in application boards and relates in particular to a functional replicator of a specific integrated circuit and its use as an emulation device when the integrated circuit is incorporated into an application board.

Background art

For a long time, the technique of silicon-based integrated circuits, which has benefited from increasingly widespread miniaturization, was dominated by so-called "standard" integrated circuits based on a central processing unit (CPU) or a microprocessor. Over the last few years, the new trend has been to use microprocessor core-based application-specific integrated circuits (ASIC) using the complex instructions set computer (CISC) or the reduced instructions set computer (RISC). Three problems occur when developing integrated circuits, whether the latter are standard or specific: emulation, which consists in replacing the integrated circuit or the chip in the final application by an emulation device performing the same functions as the integrated circuit; prototyping which consists in obtaining a prototype of the future integrated circuit, and development stage consisting in testing both the hardware and the application software and possibly performing debugging operations if problems are encountered.

The conventional approach for the emulation of integrated circuits has suffered an underlying assumption that is considered still today as an unchanging truth. The assumption is that an integrated circuit or a monolithic chip can be emulated only by another integrated circuit, that is to say, another monolithic chip that contains at least all of the functions contained in the integrated circuit that is to be emulated. The chips used for the emulation process generally contain a set of functions that were made accessible to the outside by extending the chip's inputs/outputs. These chips thus enable the emulation of all integrated circuit having functions that constitute a sub-assembly of the set of functions of the chip used for the emulation. Such chips which form the basis of the conventional emulation were indifferently referred to as the SE chip, Bound out chip, DEV chip, Emulation chip, Super chip or Piggy-Back.

Unfortunately, this conventional approach has a major drawback. As the emulation chip has only a given set of functions, it can only be used to emulate a limited number of integrated circuits. As a result, the smallest modification of the integrated circuit, other than memory size needed for the requirements of the application, may require that a new emulation chip be developed. It is thus usual to wait more than a year for an emulation circuit to be developed in order to be able to proceed with the emulation of an integrated circuit resulting from a modification of an integrated circuit that already exists, as the implementation of a new integrated circuit can only take place after its emulation circuit has been validated. This need to develop a new emulation circuit practically every time has made the development of integrated circuits very difficult and expensive, whether they are new or whether they are derived from existing integrated circuits. Furthermore, this problem has become crucial owing to the continued increase of specific integrated circuits, because it has become necessary to develop new emulation circuits very rapidly in order to meet the growing needs of specific applications and the rapid development of applications.

In order to solve the abovementioned problem, it was proposed to add to the emulation circuit a FPGA type external programmable logic array in order to incorporate a few additional functions. This solution is not adequate when a new specific integrated circuit must be created containing several peripheral functions which must be emulated in real time as the access to these functions is made by the external bus and not by the internal bus and thus at a much lower speed. Moreover, such a solution is totally inoperative when analog functions must be added to the integrated circuit.

As far as the prototyping and development of an integrated circuit are concerned, the existing solutions consist in using a set of separated boards representing the integrated circuit to be manufactured, or in using an emulation circuit previously mentioned to which one or more FPGA type programmable arrays integrating the required functions are added. This leads to making only prototypes which are much too slow and which do not represent the integrated circuit in real time or which are very close to the emulation circuit, thereby limiting the performance and the possibilities offered by these solutions due to the restricted number of functions which are traditionally found in a standard emulation circuit. It is clear that the need to develop an increasing number of specific integrated circuits for a perpetual influx of new

applications and their growing complexity has created a crucial need to have rapid and efficient development and prototyping devices.

Summary of the invention

The main object of the invention is thus to provide a functional replicator of a specific integrated circuit designed to emulate an integrated circuit within a specific application.

Another object of the invention is also to provide a functional replicator of a specific integrated circuit that can be used as a prototyping device for the integrated circuit.

Yet another purpose of the invention is also to provide a functional replicator of a specific integrated circuit that can be used as a development platform for the integrated circuit.

The invention relates therefore to a real-time functional replicator of a specific integrated circuit consisting of a processing unit and peripherals for performing specific digital and/or analog functions under the control of specific software, this specific integrated circuit being designed to be incorporated into a given application board. The device includes a processing module which is functionally identical to the processing unit of the specific integrated circuit, a plurality of peripheral modules each of which is capable of executing one or more digital and/or analog functions which can each be selected separately, and function interconnection means for establishing the connections between the processing module and the pre-selected digital and/or analog functions located in at least one of the peripheral modules, identical to the specified functions of the specific integrated circuit, such that the replicator behaves in the same manner as the specific integrated circuit when the specific software is run.

Brief description of the drawings

The objects, features and advantages of the invention will become more apparent from the following detailed description with reference to the drawings in which:

Figure 1 is a block diagram representing the functional replicator according to the invention as well as the other components needed to make it operate as an emulation, prototyping or development device,

Figure 2 represents a flowchart of the steps needed for the implementation of the functional replicator according to the invention, as an emulation, prototyping or development device,

Figure 3 is a time-based diagram showing the various phases which come into play in the fabrication and development of an application board when the prior art technique is used, and

Figure 4 is a time-based diagram showing the various phases that come into play in the development of an application board when the functional replicator according to the invention is used.

Detailed description of the invention

As shown in figure 1, the functional replicator 10 according to the invention primarily includes a processing module 12 connected to peripheral modules 14, 16 or 18 by means of a function interconnection module 20, as well as to an input/output interconnection module 22 at the output of the peripheral modules and an interface 24 which allows the functional replicator to be connected to the application board 26.

The processing module 12 is a conventional central processing unit (CPU type), generally in the form of a silicon chip, although not having the functions that are normally an integral part of an integrated circuit. All of the internal connections that are normally built into the integrated circuit take the form of external connections here, represented globally by the bus 28, referred to hereinafter as the internal bus. Therefore, the processing module 12 occupies a much larger place than the chip which will contain the specific integrated circuit which is functionally reproduced, as it features many more connections to the outside (approximately 400) than the final chip (approximately 150).

The peripheral modules are integrated circuits containing, on a single chip, a plurality of functions that can be implemented in a specific integrated circuit. The modules are divided into two categories: non-programmable (NP) modules, such as modules 14 or 16, and programmable modules (PROG) such as module 18. The non-programmable modules are circuits each having several tens of digital and/or analog functions. Classic digital functions are, for example: a time pulse generator or Timer, a USART (Universal Synchronous Asynchronous Receiver Transmitter) function, or the ADC specific function that is a communication protocol used in industry and in the automotive sector. For example,

conventional analog functions are analog-digital converters (ADC) or digital-analog converters (DAC), operational amplifiers or analog comparators. The device according to the invention provides a number of such functions in order to accommodate all functions possible to allow the specific integrated circuit to be adapted to the targeted application and to evolve with the applications, since the device according to the invention can be reprogrammed at will so that it corresponds to a new application. As for the programmable modules, they are generally provided with the expected digital functions through the programming of FPGA type programmable logic arrays.

Function interconnection means such as an interconnection matrix within a module 20 can be programmed to connect, through the first connection bus 30, the lines of the internal bus 28 to certain functions of at least one of the peripheral modules 14, 16 or 18 corresponding to the functions that will be built into the final integrated circuit. Note that the interconnection means can be integrated in the peripheral modules rather than included in a standalone module.

The input/output interconnection module 22 is an interconnection matrix programmed in the same way as the function interconnection means to connect the outputs of the functions selected in the peripheral modules using a second connecting bus 32, to the output bus 34. The output bus 34 may be connected to the application board using a ribbon cable 36 and an interface circuit 24. In fact, the ribbon cable 36 is connected to the output connections of the built-in circuit 27 that was not yet incorporated onto the board 26 (it is represented on the figure by dashed lines). This allows the device 10 to serve as an emulation device when the ribbon cable 36 is connected to the board 26.

The functional replicator 10 is connected to a host computer 38 by a JTAG type serial interface 40 that allows the computer code to be downloaded to the processing module for software testing and debugging.

For each specific integrated circuit to be emulated, the functional replicator must be configured to identically reproduce the functions of the integrated circuit. To accomplish this, an HDL (Hardware Description Language) program is developed according to the functions to be selected. The code obtained, supplied by the host computer 38, is stored in a Flash type memory 42. Then, by using the memorized code, a programmable automaton 44 performs the series/parallel conversion of the code and begins programming the configuration by activating

the appropriate connections in interconnection module 20 first, then in interconnection module 22.

The functional replicator 10 also features a memory module 43 and a ROM emulation module 45, both of which are connected to the processing module 12. The memory module is used to store the software which will be used for the application and which is transmitted to the processing module 12.

The ROM emulation module 45 is used to offset the problem resulting from the fact that it is difficult to use the memory module 43 to emulate the ROM of the integrated circuit inasmuch as the access time is not the same and the width of the memory bus (16-bit) is different from the 32-bit width used internally. As a result, the module 45 is an SSRAM memory having the same type of access as the ROM (32-bit and fixed address) with the same access time (1 cycle in read mode). A signal allows booting on the module 45, which enables the exact operating conditions of the future ROM to be reproduced and thus to validate the entire software before recording it definitively in the silicon, thereby reducing the risks involved in creating a specific integrated circuit with ROM.

Finally, a logic analyzer 46 may be connected to the internal bus 28 through a first exterior bus 48 and to the output bus 34 through a second exterior bus 50. During the test phases, the logic analyzer 46 is used to check that the function replicator 10 and the board 26 are operating correctly in terms of both the hardware and the software.

The connections of the logic analyzer with the functional replicator 10 allow all of the signals that normally exit the integrated circuit to be correlated. Furthermore, the split architecture of the device 10 also allows the signals internal to the circuit on the internal bus 28 to be monitored and thus to see all of the interactions in real time between the code, the input/output interconnection module 22 and numerous internal signals such as interruptions of the modules and the peripheral bus, etc.

The implementation of the functional replicator according to the invention, for which the various steps are shown by the flow chart in figure 2, begin with the definition and the selection of the functions (60) which are to be incorporated into the specific integrated circuit to be made. Selecting the non-programmable peripheral modules containing the desired functions makes this selection. The question remains, however, to know if these functions are all contained in the MP modules (62). If this is not the case, the missing functions must be

added by programming one or more FPGA modules (64). This programming operation is generally made using a controller that programs the functions of the FPGA module when it is turned on owing to the code that was developed beforehand in a workstation.

When the functions have been selected, the next step entails establishing the HDL language programming (66) which will enable the desired configuration to be obtained, as a result of the previous function selection. The code obtained is stored in flash memory 42. This code is used to carry out the assembly of modules of the functional replicator by being run by the controller 44 that configures the function interconnection module (68).

The next step consists in determining if we want to use the device as a prototyping device (70) to obtain a specific integrated circuit prototype. If so, the bits are loaded into the processing module 12 by means of the host computer 38 (72) and an appropriate test program is made (74).

The next step consists in determining if we want to use the device of the invention as a development platform (76). If so, we test at least a portion of the code that will be used in the application (78). The functional replicator according to the invention that has its own clock (not shown), its own memory 43 and its own features 14, 16, 18, is thus autonomous. It allows the application software's algorithms to be tested and the modification of its PLL allows the performances of the algorithms to be evaluated in real time. Furthermore, some functions are connected to standard outputs and thus may be stimulated by external devices such as terminals and other communication interfaces. In addition, they can be viewed on the screen of the logic analyzer.

It should be noted that when the device according to the invention is used as a prototyping device, the user (designer) runs all the functions of the peripheral modules, while, when the device is used as a development platform, the user (computer specialist) runs the software to test his/her algorithms, the interaction between the software and the integrated circuit and the software's performance.

Then, we continue to the next step that consists in configuring the input/output interconnection module (80) in order to obtain output connections that are identical to those of the integrated circuit to be built. The test allows us to determine if the input/output interconnection module is optimized (82). If not, the input/output interconnection module is configured once again with the parameters corrected on the basis of the test performed.

When the input/output interconnection module is optimized, the functional replicator is connected to the application board (84). Then the board and application code are tested (86) before fabrication of the specific integrated circuit is launched (88). It should be noted that this fabrication process might be undertaken at an earlier stage, once the configuration has been optimized, for example.

As shown in figure 3, the conventional method of fabrication requires that the application be tested when the integrated circuit is operational, that is to say, after fabrication. The development of the application thus only begins very late in the overall process. The same is true for the software that is developed at the end of the process. Owing to the use of the functional replicator according to the invention, the length of the application board development process is considerably reduced. Indeed, as shown in figure 4, the development of the application may begin at the same time as the design of the integrated circuit without waiting for it to be fabricated as testing of the application can be started once the integrated circuit has been designed and after its functional reproduction has been validated by the device of the invention. The same is true for the software. Qualification tests are sometimes necessary as shown in figure 4, after the integrated circuit is fabricated. If the end of the development process is located in time T1 with the conventional method, the end of the same process is situated at time T2 by using the device according to the invention, time T2 which is lower than time T1 by more than 40%.

CLAIMS

1. A real time functional replicator (10) of a specific integrated circuit comprised of a processing unit and peripherals in order to perform specific digital and/or analog functions controlled by specific software, said specific integrated circuit being designed to be incorporated into a specified application board; said device being characterized in that it includes:

a processing module (12) that is functionally identical to said processing unit of said specific integrated circuit,

a plurality of peripheral modules (14, 16, 18) each able to implement one or more digital and/or analog functions, each of said functions being able to be selected separately, and

function interconnection means (20) for establishing the connections between said processing module and one ore more digital and/or analog functions previously selected and located in at least one of said peripheral modules, said functions being identical to said specific functions of said specific integrated circuit, such that said replicator behaves identically to said specific integrated circuit when said specific software is run.

2. The device according to claim 1, wherein said function interconnection means are included in a standalone module (20).

3. The device according to claim 2, in which said function interconnection module (20) is connected to said processing module (12) through a so-called internal bus (28) grouping together the internal connections of said specific integrated circuit between its processing unit and its peripherals.

4. The device according to claim 2 or 3, in which said function interconnection module (20) is configured by a programmable automaton (44) using software set up when said digital and/or analog functions, which must be implemented by said peripheral modules (14, 16, 18), have been selected.

5. The device according to claim 1, wherein said interconnection means are integrated within said peripheral modules (14, 16, 18).

6. The device according to any one of claims 1 to 5, in which said peripheral modules feature one or more integrated circuits (14, 16) each of which are specially designed to implement a plurality of digital and/or analog functions.

7. The device according to claim 6, in which said peripheral modules also include one or more FPGA type programmable logic arrays (18) which were previously programmed to implement at least one digital function which is not implemented by said integrated circuits (14, 16) specially designed to implement the digital and/or analog functions.

8. The device according to claim 7, featuring an input/output connection module (22) and an interface (24) connected to said input/output interconnection module by an input/output bus (34) and which can be connected to the input/output pins of the specific integrated circuit in the specified application board, said input/output interconnection module establishing the connections between the outputs of the digital and/or analog functions previously selected of said peripheral modules (14, 16, 18) and said interface.

9. The device according to claim 7 or 8, in which said input/output interconnection module (22) is configured by said programmable automaton (44) by means of said software set up when said digital and/or analog functions were selected.

10. The device according to any one of claims 1 to 9, further including a ROM emulation module (45) connected directly to said processing module (12) to emulate the ROM memory of said specific integrated circuit, said ROM emulation module preferably being a SSRAM memory, having the same type of access and the same access time as said ROM memory.

11. The device according to claim 10, used as an emulation device of said specific integrated circuit when said interface (24) is connected, for example, using a ribbon cable (36), to the input/output pins of said specific integrated circuit (27) designed to be built into said specified application board (26).

12. The device according to any one of claims 1 to 7, used as a prototyping device to implement a prototype of said specific integrated circuit (27) designed to be built into said specific application board (26).

13. The device according to any one of claims 1 to 7, used as a development platform for said specific integrated circuit (27) designed to be built into said specified application board (26).

Functional replicator of a specific integrated circuit and its use as an emulation device

Abstract

A real time functional replicator (10) of a specific integrated circuit comprised of a processing unit and peripherals in order to perform specific digital and/or analog functions controlled by specific software, this specific integrated circuit being designed to be incorporated into a specified application board. Such a device includes a processing module (12) that is functionally identical to the processing unit of the specific integrated circuit, a plurality of peripheral modules (14, 16, 18) each able to implement one or more digital and/or analog functions, each of the functions being able to be selected separately, and function interconnection means (20) for establishing the connections between the processing module and one ore more digital and/or analog functions located in at least one of the peripheral modules which are identical to the specific functions of the specific integrated circuit, such that the replicator behaves identically to the specific integrated circuit when the specific software is run.

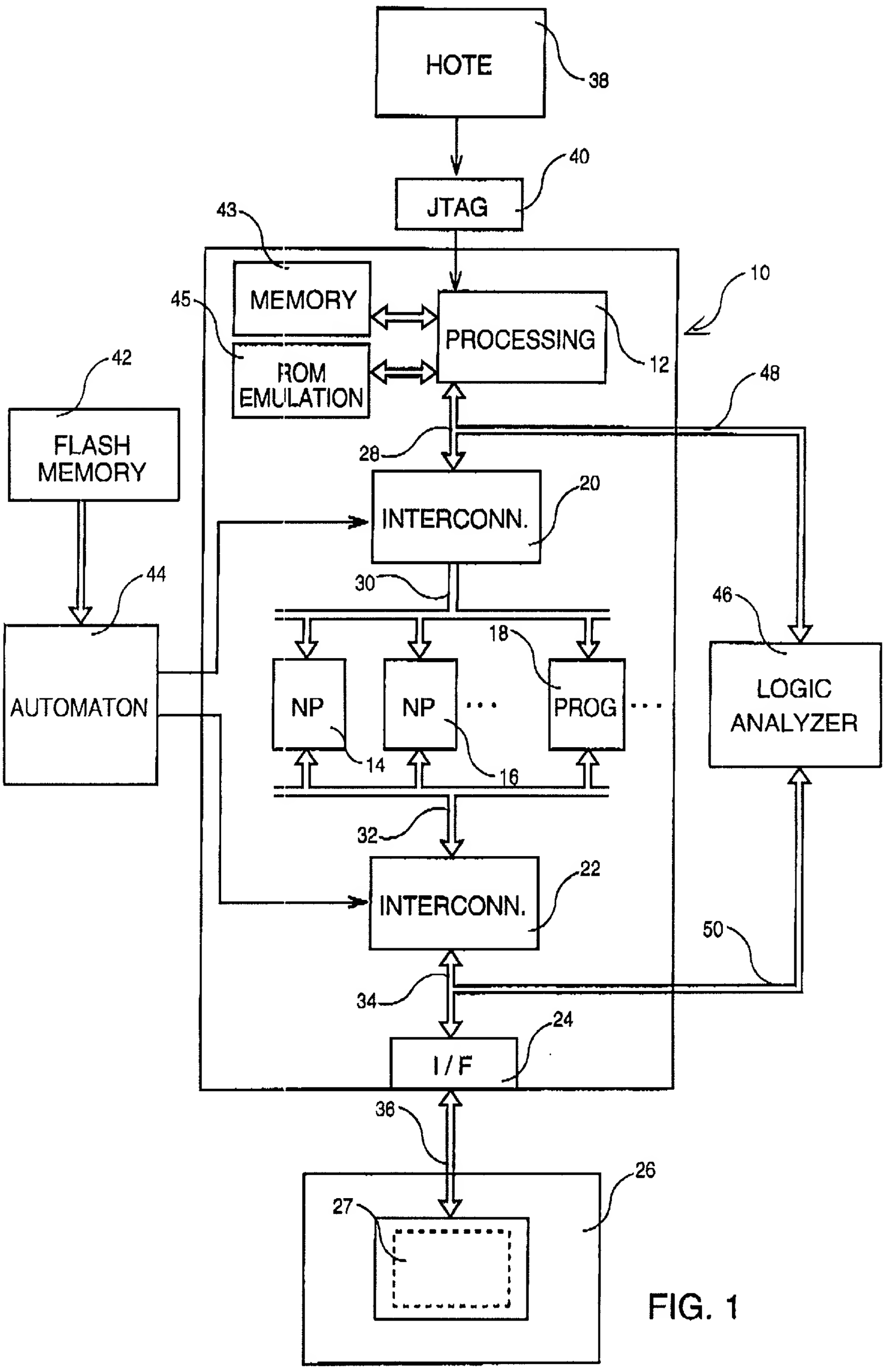
HOTE
38
40
JTAG
43
MEMORY
45
ROM EMULATION
PROCESSING
12
10
42
FLASH MEMORY
48
28
INTERCONN.
20
44
AUTOMATON
30
46
18
NP
NP
PROG
LOGIC ANALYZER
14
16
32
INTERCONN.
22
50
34
24
I/F
36
26
27

FIG. 1

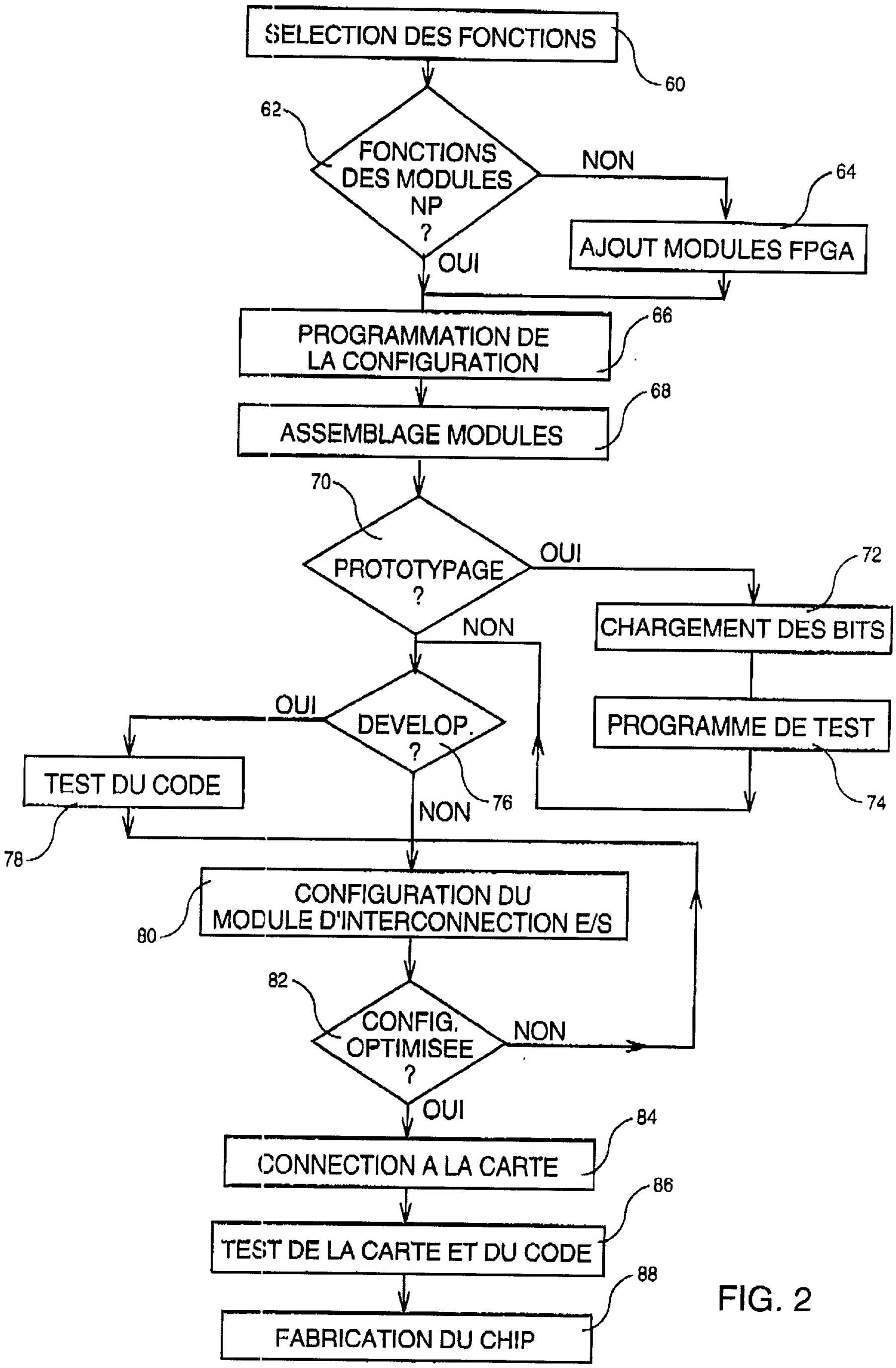
SELECTION DES FONCTIONS
60
62
FONCTIONS DES MODULES NP ?
NON
64
AJOUT MODULES FPGA
OUI
PROGRAMMATION DE LA CONFIGURATION
66
ASSEMBLAGE MODULES
68
70
PROTOTYPAGE ?
OUI
72
CHARGEMENT DES BITS
NON
OUI
DEVELOP. ?
PROGRAMME DE TEST
TEST DU CODE
76
74
NON
78
CONFIGURATION DU MODULE D'INTERCONNECTION E/S
80
82
CONFIG. OPTIMISEE ?
NON
OUI
84
CONNECTION A LA CARTE
86
TEST DE LA CARTE ET DU CODE
88
FABRICATION DU CHIP

FIG. 2

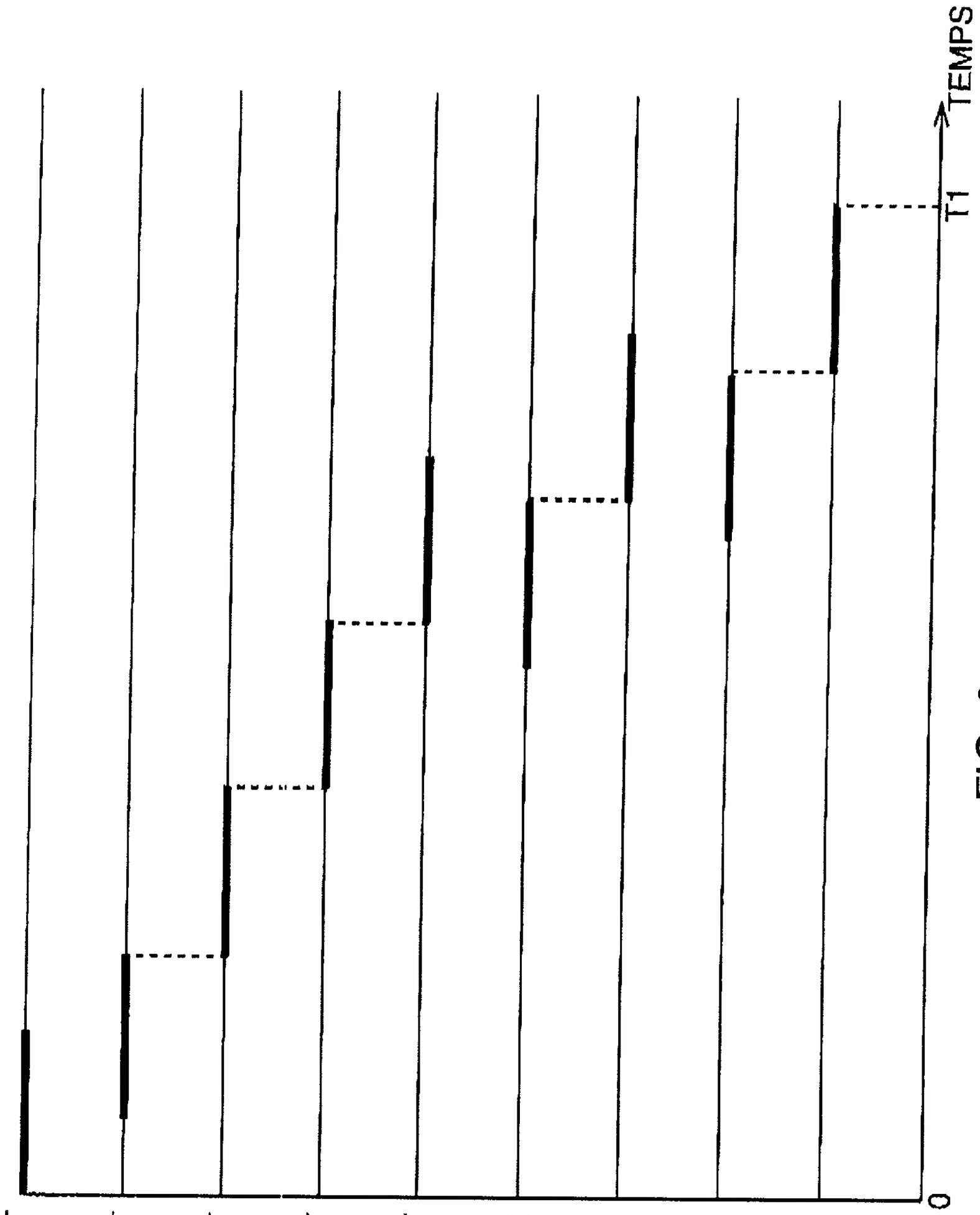
TEMPS
T1
DESIGN DU CIRCUIT
TEST THEORIQUE DU CIRCUIT
CONCEPTION PHYSIQUE DU CIRCUIT
FABRICATION DU CIRCUIT
TEST PHYSIQUE DU CIRCUIT
REALISATION DE L'APPLICATION
TEST DE L'APPLICATION
REALISATION DU LOGICIEL
TEST DU LOGICIEL
0

FIG. 3


TEMPS
T2
0
DESIGN DU CIRCUIT
TEST THEORIQUE DU CIRCUIT
CONCEPTION PHYSIQUE DU CIRCUIT
FABRICATION DU CIRCUIT
TEST PHYSIQUE DU CIRCUIT
REALISATION DE L'APPLICATION
TEST DE L'APPLICATION
REALISATION DU LOGICIEL
TEST DU LOGICIEL

FIG. 4

SMALL ENTITY DECLARATION

APPLICANT OR PATENTEE EUROPE TECHNOLOGIES S.A.

SERIAL NO. _____ ☐ PATENT NO _____ DOCKET NO. BONN-039

(Check one of blocks 1 or 2)

1. ☐ FILED OR ISSUED _____
2. ☒ SUBMITTED HEREWITH _____

FOR Functional replicator of a specific integrated circuit and its use as an emulation device
(Insert Title)

I(we) hereby declare that I(we) am(are) entitled to the benefit of small entity status with respect to the above-identified application or patent for purposes of paying reduced fees under 35 USC 41(a) & (b) to the U.S. Patent and Trademark Office.

☐ A. INDEPENDENT INVENTOR
I(we) qualify as (an) independent inventor(s) as defined in 37 CFR 1.9(c).

☐ B. INDIVIDUAL NON-INVENTOR
I would qualify as an independent inventor as defined in 37 CFR 1.9(c) if I had made the invention.

☒ C. SMALL BUSINESS CONCERN
I am ☐ THE OWNER ☐ AN OFFICIAL of the small business concern identified below and am empowered to act on behalf of the concern. The concern qualifies under 37 CFR 1.9(d) and 13 CFR 121.1301-1305. Rights under contract or law have been conveyed to and remain with the concern and are exclusive unless a checkmark is placed here ☐. All other rights belong to small entities as defined in 37 CFR 1.9.

☐ D. NON-PROFIT ORGANIZATION
I am an official am empowered to act on behalf of the non-profit organization identified below. The organization qualifies under 37 CFR 1.9(e), sub section: ☐ (1) ☐ (2) ☐ (3) ☐ (4). Rights under contract or law have been conveyed to and remain with the organization and are exclusive unless a checkmark is placed here ☐ All other rights belong to small entities as defined in 37 CFR 1.9.

I(we) acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b)).

I(we) declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

A. INDEPENDENT INVENTOR(S)

Name _____ Signature _____ Date _____

Name _____ Signature _____ Date _____

Name _____ Signature _____ Date _____

B. INDIVIDUAL NON-INVENTORS

C. BUSINESS CONCERN

EUROPE TECHNOLOGIES S.A.
Name of Concern or Organization

Sghaier NOURY
Name of Person Signing

C.E.O.
Title

D. NON-PROFIT ORGANIZATION

Les Taissounières HB3
Address 1681, Route des Dolines
06560 SOPHIA ANTIPOLIS - FRANCE

Signature S.NOURY

Date 18/10/00

Docket No. BONN-039

Declaration For U.S. Patent Application

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled (INSERT TITLE) Functional replicator of a specific integrated circuit and its use as an emulation device, the specification of which

(Check one of 1, 2, or 3.)

1. X is attached hereto.
2. __ was filed on _____ as International PCT Application Serial No. _____ and was amended on _____ (if applicable).
3. __ was filed on _____ as U.S. Application Serial No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above.

I acknowledge the duty to disclose all information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application for which priority is claimed:

(List prior foreign applications.)

(Number)	(Country)	(Day/Month/Year Filed)	Priority Claimed
00480051.2	EUROPE	16/06/2000	X Yes __ No
			__ Yes __ No

__ See attached list for additional prior foreign applications

I hereby claim the benefit under Title 35, United States Code, §120, of any United States application listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56, which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status)

I hereby appoint as principal attorney James C. Lydon, Reg. No. 30,082.

Please direct all communications to the following address:

James C. Lydon
Attorney at Law
100 Daingerfield Road, Suite 100
Alexandria, Virginia 22314
Telephone: (703) 838-0445
Facsimile: (703) 838-0447

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first or sole inventor: Sghaier NOURY

Inventor's Signature: _____ Date: 18/10/2000

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Citizenship: French

Post Office Address: same as residence

Full name of second inventor: Tristan BONHOMME

Inventor's Signature: _____ Date: 15/10/2000

Residence: Les Bleuets B3 - Rue Max Jacob - 06600 ANTIBES - FRANCE

Citizenship: _____

Post Office Address: same as residence

Full name of third inventor: Pascal JULLIEN

Inventor's Signature: _____ Date: 15/10/2000

Residence: Residence les Vergers F - 1978 Avenue de Provence - 06140 VENCE - FRANCE

Citizenship: _____

Post Office Address: same as residence

Full name of fourth inventor: _____

Inventor's Signature: _____ Date: _____

Residence: _____

Citizenship: _____

Post Office Address: _____

Full name of fifth inventor: _____

Inventor's Signature: _____ Date: _____

Residence: _____

Citizenship: _____

Post Office Address: _____

Full name of sixth inventor: _____

Inventor's Signature: _____ Date: _____

Residence: _____

Citizenship: _____

Post Office Address: _____

Full name of seventh inventor: _____

Inventor's Signature: _____ Date: _____

Residence: _____

Citizenship: _____

Post Office Address: _____

Full name of eighth inventor: _____

Inventor's Signature: _____ Date: _____

Residence: _____

Citizenship: _____

Post Office Address: _____